UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,763	01/31/2006	Godefridus Johannes Gertrudis Maria Geelen	NL03 0935 US1	6167

65913 7590 07/14/2008

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
CHENG, DIANA	

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
07/14/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/566,763	GEELEN, GODEFRIDUS JOHANNES GERTRUDIS M	
	Examiner	Art Unit	
	DIANA J. CHENG	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4 and 6-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4 and 6-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments, see Page 4, filed 12/24/2007, with respect to 35 U.S.C. 112, second paragraph of claim 6, have been fully considered and are persuasive. The rejection of claim 6 has been withdrawn.

2. Applicant's arguments filed 12/24/2007 have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 3, 4, 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dedic (5,384,570), and in view of Fig. 2 as depicted in applicant admitted prior art (AAPA).

Re claim 1, Dedic discloses a single track-and-hold circuit in Fig. 11 having an input (Vin) [Vi] and an output signal (Vs) [Vo], a bootstrap switch (14a) [4] having as its inputs a clock signal [CK] and an input signal (vin) [Vhigh], said input signal (vin) [Vhigh] of said bootstrap switch (14a) being connected to said output signal (Vs) [Vo] of said circuit via level shifting (20) [Fig. 2, 33; Fig. 4, cascoded source follower 31] and buffering means (30) [Fig. 2, 32; Fig. 4, a current source 32], characterized in that said input signal (vin) of said bootstrap switch (14a) [4, 5] comprises said output signal (Vs) [Vo] of said circuit [Vo is connected to 4]; said single track-and-hold circuit further comprises a capacitor (12) [2], said input signal being connected to said capacitor (12) via a switch (10) [Vi through 1 to 2], said switch (10) [1] being closed during a track mode of said circuit and open during a hold mode of said circuit [Col. 1, lines 14-30],

said bootstrap switch (14a) including two or more bootstrap switches (14a, 14b) [4,5 included in VSC1, VSC2], the input signal (vin) of each of which is connected to said output signal (Vs) [Vo] of said circuit via said level shifting (20) [Fig. 7, where in 31, L1 and L2 are connected to 4,5] and buffering means (30) [32] of said single track-and-hold circuit, but does not teach the details of output of the bootstrap circuit.

AAPA does in Fig. 2, and in more detail on page 1 of specification, lines 18-19, where said bootstrap switch (14a) having as an output to said switch (10), a clock signal (clkboot) equal to said input signal (Vin) added to a supply voltage (Vdd). ("Vclkboot_high = vin + VDD"). The AAPA The AAPA teaches in detail in Fig. 2 the characteristics of the output of the bootstrap circuit, in particular on page 1, lines 14-20, where it is disclosed that "Vclkboot_high = Vin + Vdd".

Therefore, it would be obvious to one of ordinary skill in the art to use the detailed teachings of the AAPA to further describe the bootstrap circuit disclosed in Dedic for the purpose of providing further circuitry details.

Re claim 3, Dedic and AAPA, as a whole, teach single a track-and-hold circuit according to the present invention, wherein said buffering means (30) comprises a MOS transistor [Fig. 2, 33; Fig. 4, 31].

Re claim 4, Dedic and AAPA, as a whole, teach a single track-and-hold circuit according to the present invention, wherein said MOS transistor (30) is a PMOS transistor [Fig. 4, 33, 34].

Re claim 8, Dedic and AAPA, as a whole, teach an analog-to-digital converter including a single track-and-hold circuit according to the present invention [Col. 1, lines 6-9].

Re claim 9, Dedic and AAPA, as a whole, teach an integrated circuit including an analog-to-digital converter according to the present invention [where it would be inherent for an analog-to-digital converter be used in an integrated circuit].

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dedic (5,384,570) and Fig. 2 as depicted in applicant admitted prior art (AAPA), as a whole, as applied to claim 1 above, and further in view of Jensen et al. (US 2002/0084808 A1)

Re claim 6, Dedic and AAPA, as a whole, teach single a track-and-hold circuit according to the limitations of the present invention, but does not teach the rest of the claim.

Jensen et al. teaches a single track and hold circuit in Fig. 2 further comprising one or more dummy switches (16) [56 and 58] which are clocked in anti-phase [A#] to said switch (10) [52, 54] connecting said input signal (Vin) [INPUT] to said capacitor (12) [46].

Dedic and AAPA, as a whole, and Jenson et al. both teach a single track and hold circuit. Jenson further teaches the use of cancellation transistors, which are equivalent to dummy transistors. In [0008], Jenson et al. teaches "one or more 'cancellation' transistors are employed within the switch circuit to dump charge of an opposite polarity (e.g., negative charge rather than positive charge) onto the circuit node at approximately the same time to reduce or eliminate the effects of the charge dumped by the switching transistors." Therefore, it would be obvious to improve the single track and hold circuit of Dedic and AAPA, as a whole, to further include the cancellation transistors as taught by Jenson et al, in order to eliminate the effects of the charge dumped by the switching transistors.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dedic (5,384,570) and Fig. 2 as depicted in applicant admitted prior art (AAPA), and Jensen et al. (US 2002/0084808 A1), as a whole, as applied to claim 6 above, and further in view of Fig. 3 as depicted in applicant admitted prior art (AAPA).

Re claim 7, Dedic, AAPA, and Jenson et al., as a whole, teach a single track-and-hold circuit according the limitations of the present invention, but does not teach the rest of the claim.

The AAPA further teaches in Fig. 3 the single track and hold circuit wherein said input signal (Vin) is connected to said dummy switches (16) via a bootstrap switch (14b), having as an additional input an anti-phase clock signal.

Dedic, AAPA, and Jenson et al., as a whole, teach A# input into the dummy switches but do not where it is inputted from. Fig. 3 of AAPA does though. As stated on Page 1 of the specification in lines 21-26, "a well known solution to this is to use dummy switches." Therefore, it would be obvious to one of ordinary skill in the art to use a second bootstrap circuit of the AAPA, as shown in Fig. 3 to supply the A# input, in addition to the circuitry as taught in Dedic, Fig. 2 of AAPA, and Jenson et al, as a whole.

Response to Arguments

Applicant states on pages 4 and 5 of Remarks, "Applicant asserts that claim 1, as amended, is not unpatentable over Dedic in view of the AAPA because neither Dedic nor the AAPA teach or suggest two or more bootstrap switches, "the input signal (vin) of each of which is connected to said output signal (Vs) of said single track-and-hold circuit

via said level shifting (20) and buffering means (30) of said single track-and-hold circuit." The Office action cites "Fig. 11, 4, 5 included in VSC 1, VSC2" of Dedic as teaching two or more bootstrap switches as recited in amended claim 1. Applicant respectfully points out that VSC 1 and VSC2 in Fig. 11 of Dedic represent two separate voltage storage circuits, Dedic col. 25, lines 46 - 48. Although Fig. 11 depicts two bootstrap switched driving devices (4, 5), the two bootstrap switched driving devices (4, 5) are each associated with a different one of the two separate voltage storage devices, VSC1 and VSC2. In contrast to Dedic, amended claim 1 recites a single track-and- hold circuit that includes two or more bootstrap switches. In particular, amended claim 1 recites two or more bootstrap switches, "the input signal (vin) of each of which is connected to said output signal (Vs) of said single track-and-hold circuit via said level shifting (20) and buffering means (30) of said single track-and-hold circuit." Clearly the two bootstrap switched driving devices (4,5) depicted in Fig. 11 of Dedic are not connected to the output signal via the same level shifting and buffering means as recited in amended claim 1. Because Dedic does not teach or suggest the above-identified limitation of amended claim 1, Applicant asserts that a prima facie case of obviousness has not been established.

Examiner respectfully disagrees. As shown in Fig. 11, the two circuits VSC1 and VSC2 are connected to each other and to the input and output of the circuit through S1-S5. Therefore, a single track-and-hold circuit is taught.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DIANA J. CHENG whose telephone number is (571)270-1197. The examiner can normally be reached on Monday-Friday, 9 am-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew N. Richards can be reached on (571) 272-1736. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T. Lam/
Primary Examiner, Art Unit 2816

/Diana J Cheng/
Examiner, Art Unit 2816
07/08/2008